

-- REMARKS --

The present amendment replies to an Office Action dated July 22, 2008. Claims 1-18 are pending in the present application. Claims 1, 9, 11, 17, and 18 have been amended herein. In the Office Action, the Examiner rejected claims 1-18 on various grounds. The Applicants respond to each ground of rejection as subsequently recited herein and requests reconsideration of the present application.

Claim Objections

Claim 9 was objected to for including "further" at line 1. Claim 9 has been amended herein to delete "further" and not to avoid any cited reference. Withdrawal of the objection to claim 9 is respectfully requested.

35 U.S.C. §102 Rejections

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the . . . claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Thus, to warrant the §102 rejection, the references cited by the Examiner must show each and every limitation of the claims in complete detail. The Applicants respectfully assert that the cited references fail to do so.

A. Claims 1-18 were rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 5,872,429 to Xia, *et al.* (the *Xia* patent).

The Applicants respectfully assert that the *Xia* patent fails to disclose, teach or suggest each and every element of the Applicants' invention as claimed, as required to maintain a rejection under 35 U.S.C. §102(b). The *Xia* patent fails to disclose:

A ballast (10) receiving line voltage, including an inverter output stage (30); and a power factor correction input stage (20) receiving said line voltage and being in electrical communication with said inverter output stage (30) to apply a regulated DC voltage to said inverter output stage (30), said regulated DC voltage being a function of said line voltage,

said power factor correction input stage (20) including a power factor correction integrated circuit (26), and a line voltage sensing circuit (22) in electrical communication with said power factor correction integrated circuit (26) to apply a clamped rectified voltage to said power factor correction integrated circuit (26), wherein said clamped rectified voltage is a function of a load being applied by said inverter output stage (30) to said power factor correction integrated circuit (26), as recited in independent claim 1;

A power factor correction input stage (20) receiving line voltage, including a power factor correction integrated circuit (26); a line voltage sensing circuit (22) in electrical communication with said power factor correction integrated circuit (26) to apply a clamped rectified voltage as a function of said line voltage to said power factor correction integrated circuit (26), wherein the clamped rectified voltage is a function of a load being applied to said power factor correction integrated circuit (26), as recited in independent claim 11;

A ballast (10) receiving line voltage, including an inverter output stage (30); and a power factor correction input stage (20) receiving said line voltage and being in electrical communication with said inverter output stage (30) to apply a regulated DC voltage as a function of said line voltage to said inverter output stage (30), said power factor correction input stage (20) including a power factor correction integrated circuit (26), and means for applying a clamped rectified voltage to said power factor correction integrated circuit (26), wherein said clamped rectified voltage is a function of a load being applied by said inverter output stage (30) to said power factor correction integrated circuit (26), as recited in independent claim 17;

A power factor correction input stage (20) receiving line voltage, including a power factor correction integrated circuit (26); means for applying a clamped rectified voltage as a function of said line voltage to said power factor correction integrated circuit (26), wherein the clamped rectified voltage is a function of a load being applied to said power factor correction integrated circuit (26), as recited in independent claim 18.

At most, the *Xia* patent discloses receiving 120 V, 60 Hz AC input at terminals 1', 2'. *See* Figure 2a; column 6, lines 49-51. Output voltage regulation is accomplished by the sensing of the scaled output voltage, from the divider formed by the resistors R14, R15, by

the internal error amplifier at the INV pin. The internal error amplifier compares the scaled output voltage to an internal reference voltage, and generates an error voltage. This error voltage controls the amplitude of the multiplier output, which adjusts the peak inductor current in winding 52 to be proportional to load and line variations, thereby maintaining a well regulated output voltage for the inverter circuit E. For a 120 V AC input, without phase cutting, the voltage at output 80, the positive side of buffer capacitor C10, is on the order of 300 V DC with a small alternating DC component present. *See* Figure 2a; column 8, lines 35-49. Thus, the *Xia* patent fails to disclose regulated DC voltage being a function of the line voltage or a clamped rectified voltage being a function of a load as claimed.

Claims 2-10 and claims 12-16 depend directly from independent claims 1 and 11, respectively, and so include all the elements and limitations of their respective independent claims. The Applicants therefore respectfully submit that dependent claims 2-10 and 12-16 are allowable over the *Xia* patent for at least the same reasons as set forth above for their respective independent claims.

Withdrawal of the rejection of claims 1-18 under 35 U.S.C. §102(b) as being unpatentable over the *Xia* patent is respectfully requested.

SUMMARY

Reconsideration of the rejection of claims 1-18 is requested. The Applicants respectfully submit that claims 1-18 fully satisfy the requirements of 35 U.S.C. §§102, 103, and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested.

Dated: **October 22, 2008**

Respectfully submitted,
YIMIN CHEN, *et al.*

PHILIPS INTELLECTUAL PROPERTY
& STANDARDS
P.O. Box 3001
Briarcliff Manor, New York 10510

Eric M. Bram
Registration No. 37,285
Attorney for Applicant

CARDINAL LAW GROUP
Suite 2000
1603 Orrington Avenue
Evanston, Illinois 60201
Phone: (847) 905-7111
Fax: (847) 905-7113

/FRANK C. NICHOLAS/
Frank C. Nicholas
Registration No. 33,983
Attorney for Applicant